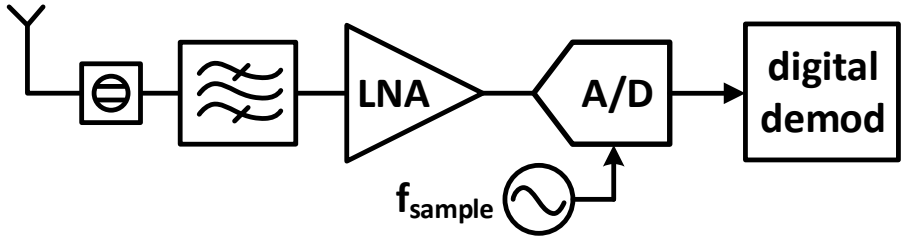
RF sampling ADCs for next generation wireless applications

Nereo Markulić on behalf on imec's ADC team

RF-sampling ADC

Direct digitization of an RF signal



"The dream of placing an ADC at the antenna"

- *Limited* analog front-end requirements
- Technology scaling friendly
- Complete flexibility over all bands

- But many challenges …
  - ADC must operate at wide bandwidth with low noise and low distortion

RF-sampling ADC

ADC requirements [current targets]

- Application in FR1 space
  - 5 GHz bandwidth
    - Up to 7 GHz with LTE-U and WiFi 6/7 networks
  - Signal-to-Noise Ratio > 56 dB [9 ENOB]
  - Spurious Free Dynamic Range > 65 dB
  - Fs > 16 Gsps
    - Some oversampling needed to
      - Reduce anti-aliasing requirements
      - Permit wide-band *frequency dependent* nonlinearity calibration
  - Medium resolution
    - 10-13b
  - Sub-1 W power

RF-sampling ADC

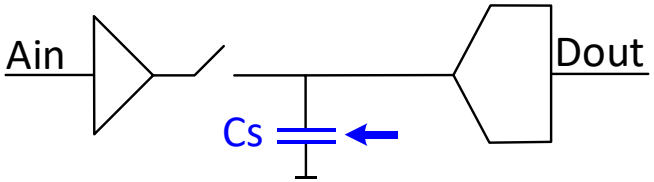
ADC requirements [future targets]

- More bandwidth! Higher clock rate! Same linearity! Same power!

- Application in FR3 space
  - 20 GHz bandwidth
  - Signal-to-Noise Ratio > 50 dB [8 enob]
  - Spurious Free Dynamic Range > 65 dB (!)
  - Fs > 32 Gsps (!)
  - Resolution 8-12b
  - Sub-1W power (!)

RF-sampling ADC

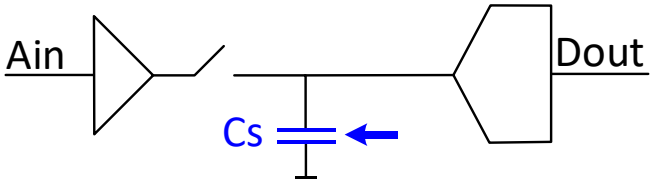
Design strategy: Front-end S&H sampling capacitor size



- Sampling capacitor size → noise vs. linearity
  - Large capacitor size reduces noise [kT/C as a fundamental limit]
  - Wide-band linearity *extremely* challenging with large loads
    - Buffering and front-end sampler are critical
    - Signal frequency dependent distortion ≠ Signal frequency independent (static) distortion
      - (Very) difficult and power costly to calibrate

RF-sampling ADC

Design strategy: Front-end S&H sampling capacitor size

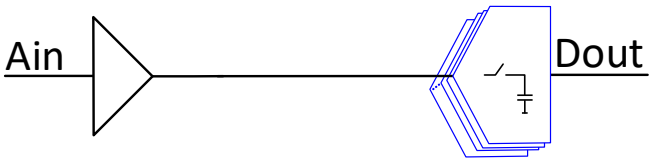


Large Cs	*Small Cs*
Low kT/C Noise	High kT/C Noise
High distortion	Low distortion

RF-sampling ADC

Design strategy: interleaving

Limited channel speed → large # of channels

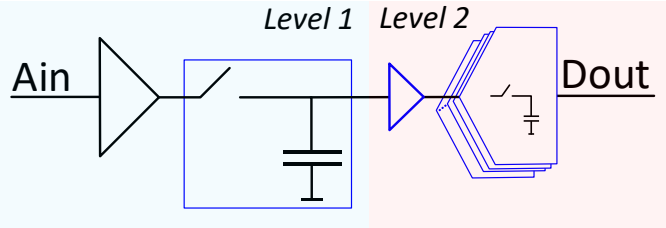


- Interleaving enables multi-GSps ADCs
- *Fast channel* permits *reduced interleaving effort*
  - Less distribution parasitics
  - Reduced calibration effort
    - Gain & Offset errors [are input signal frequency independent] → easy to correct
    - Bandwidth & Skew errors [are input signal frequency dependent] → difficult to correct
- Channel speed is limited by technology

RF-sampling ADC

Design strategy: interleaving

Hierarchy with large # of back-end channels

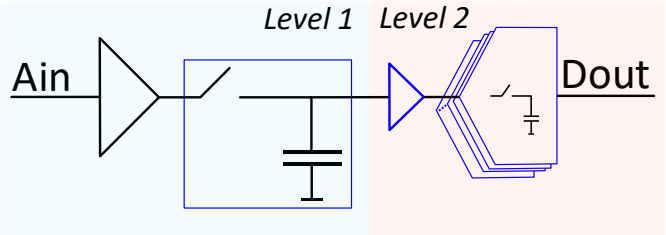


- *Direct* interleaving vs. *Hierarchical* interleaving
  - Direct interleaving is impractical when # of channels is large…
    - Large input parasitics with increased area
    - Explosion of interleaving calibration effort
  - Hierarchical interleaving reduces the problem but necessitates *rebuffering*
    - Additional power consumption
    - Noise and linearity degradation

RF-sampling ADC

Design strategy: interleaving

Hierarchy with large # of back-end channels

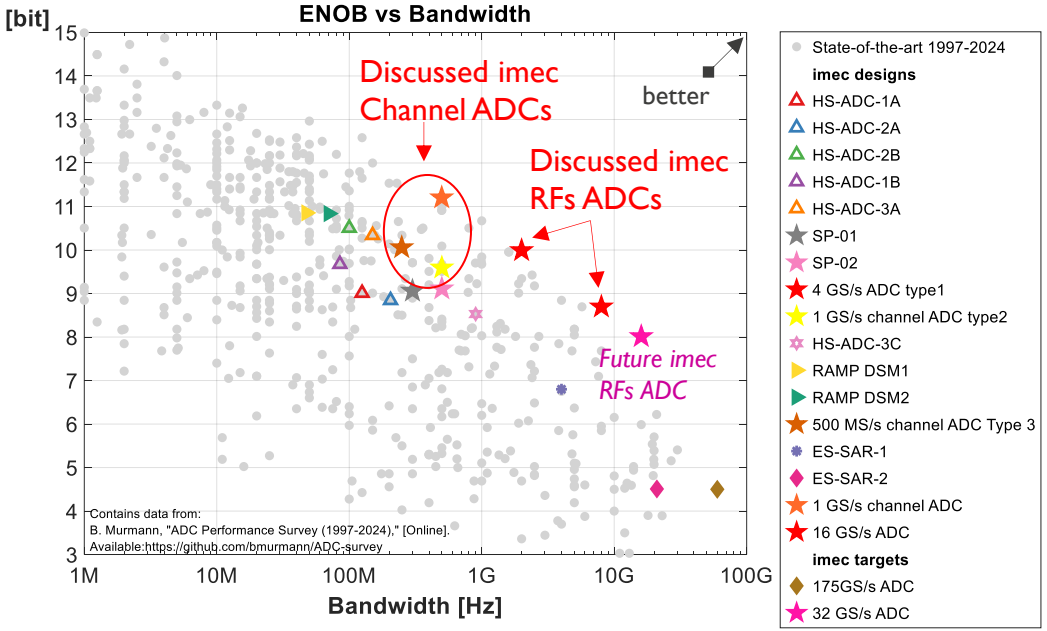


Direct	*Hierarchical*
High front-end parasitic load	Low front-end parasitic load
Large interleaving distortion	Low interleaving distortion
Good SNR-Power trade-off	Worse SNR-Power trade-off

RF-sampling ADCs

…key technology for SOTA RF-sampling ADCs covered in this talk

1. Fast & power efficient **channel**
   - Ring amplification techniques
   - Data-driven data distribution
2. Signal integrity-preserving **hierarchical architecture**
3. Wide-band linear **front-end** S&H



Key technologies:

1. Fast & power efficient channel
2. Signal integrity-preserving hierarchical architecture
3. Wide-band linear front-end buffer

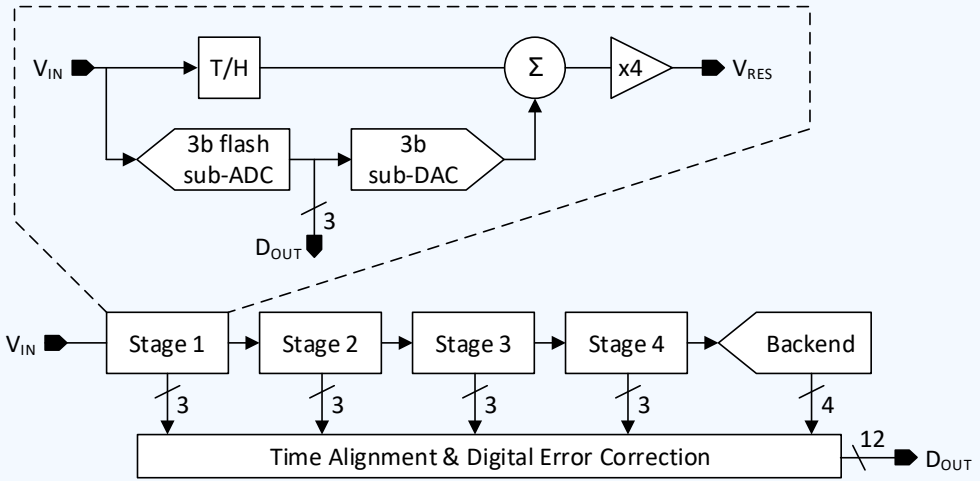
1. Fast & power efficient channel

RF-sampling ADC: fast & power efficient channel

Pipelining

- Pipelining
  - Break task into smaller pieces
  - Pass incomplete result along for more processing
  - Appears in all medium/high resolution giga-sample ADCs
- Minimize # of operations in critical timing path
  - Sample
  - Quantize
  - Amplify

Example 3b/stage Pipelined ADC



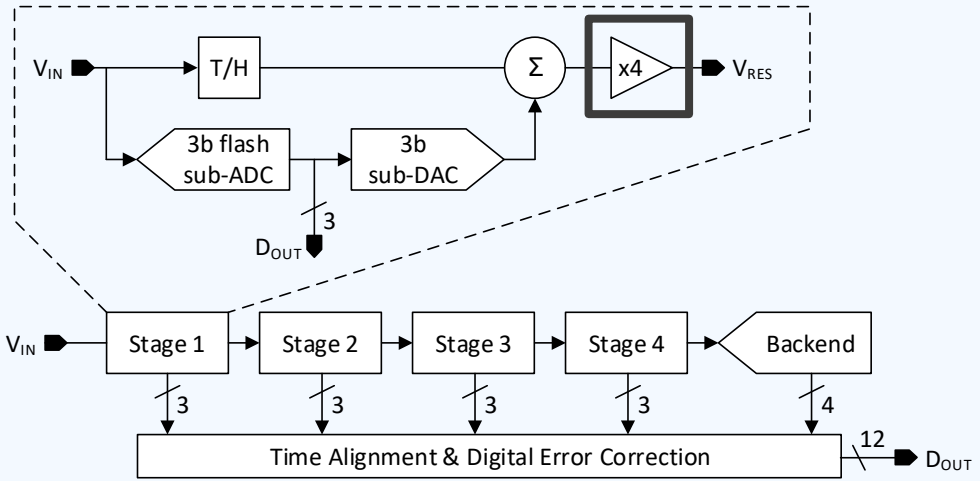
- 2b/stage of quantization
- 1b/stage of redundancy (error correction)

RF-sampling ADC: fast & power efficient channel

Residue amplification as the hidden bottleneck

- Pipelining
  - Break task into smaller pieces
  - Pass incomplete result along for more processing
  - Appears in all medium/high resolution giga-sample ADCs
- Minimize # of operations in critical timing path
  - Sample
  - Quantize
  - **Amplify ← speed & linearity bottleneck**

Example 3b/stage Pipelined ADC

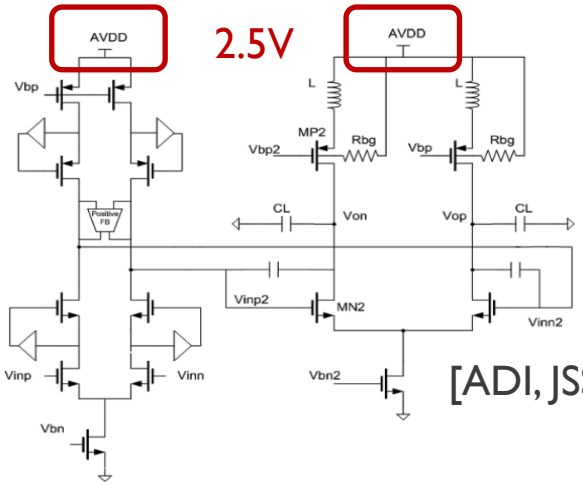


- 2b/stage of quantization
- 1b/stage of redundancy (error correction)

RF-sampling ADC: fast & power efficient channel

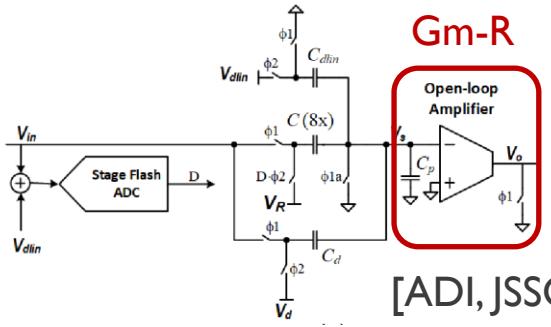
Residue amplification as the hidden bottleneck

- Class-A opamps in nanoscale CMOS
  - ☹ Not enough voltage headroom
  - ☹ Poor efficiency / technology scaling
- Requires a special high-voltage supply
  - ☹ Eliminates *all hope* of high efficiency



[ADI, JSSC 2014]

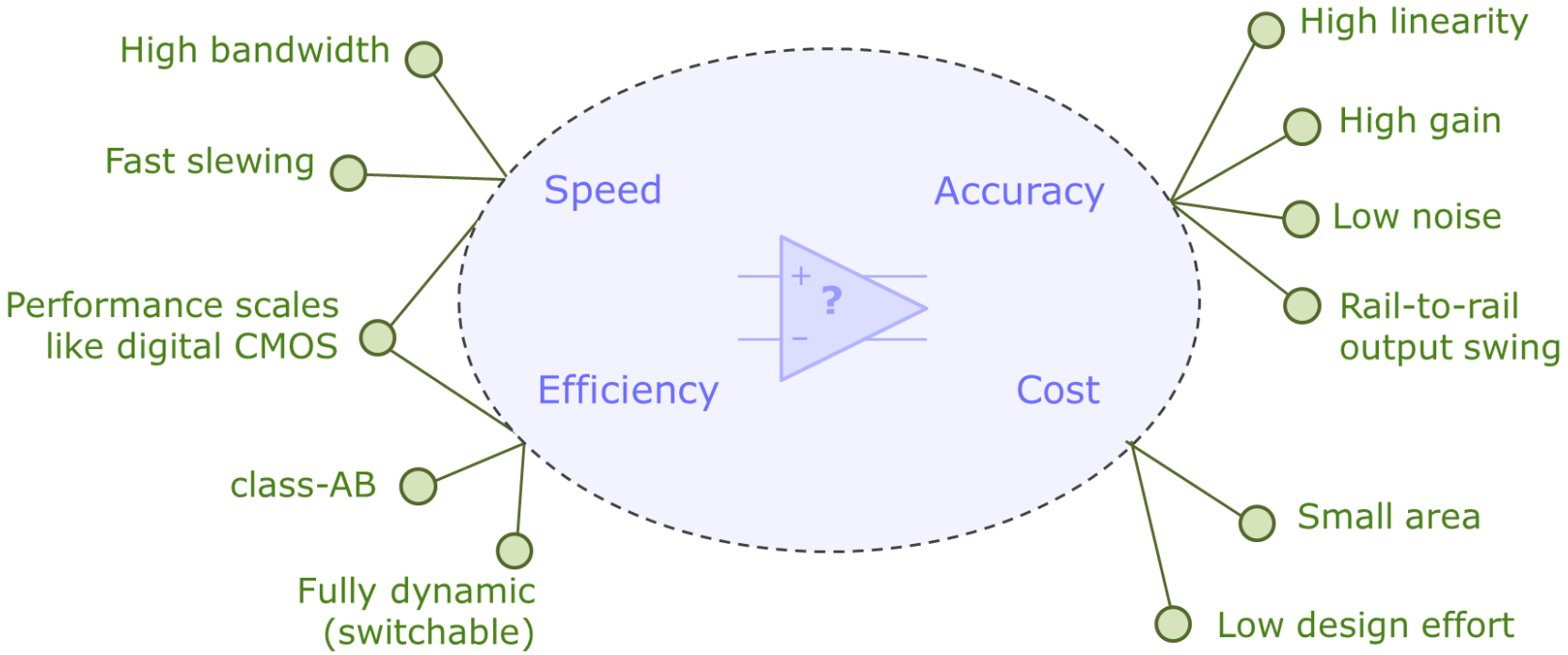
- Open loop amplifiers in nanoscale CMOS [Gm-R or Gm-C]
  - ☺ Fast and & power efficient but …
  - ☹ Need power consuming *linearization*
  - ☹ Limited voltage swing (poor SNR)



[ADI, JSSC 2018]

RF-sampling ADC: fast & power efficient channel

Ring amplifier

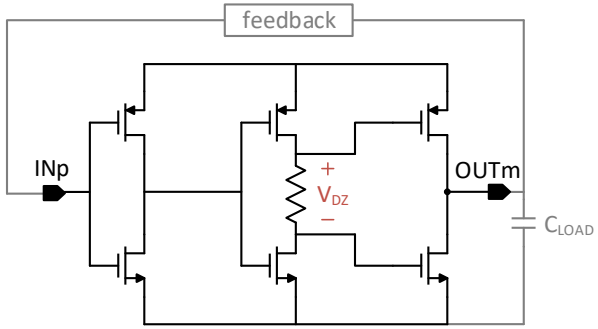


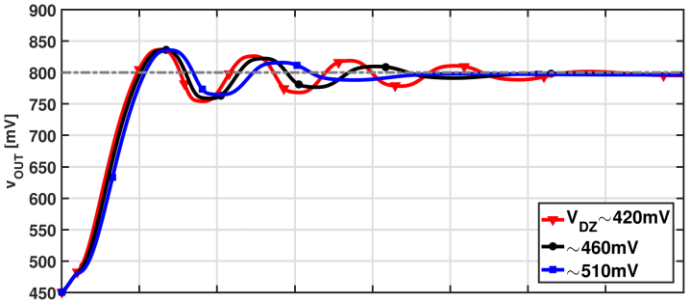
RF-sampling ADC: fast & power efficient channel

Ring amplifier

- Basic idea: Stabilize by dynamically forming a dominant output pole [Hershberg, JSSC 2012]
  - ☺ High efficiency
  - ☺ High speed
  - ☺ Wide output swing
  - ☺ Excellent linearity
  - ☺ Scales with digital
  - ☺ Fully dynamic (switchable)
  - 😐 Moderate PVT sensitivity

[Lim, JSSC 2015 (1)]



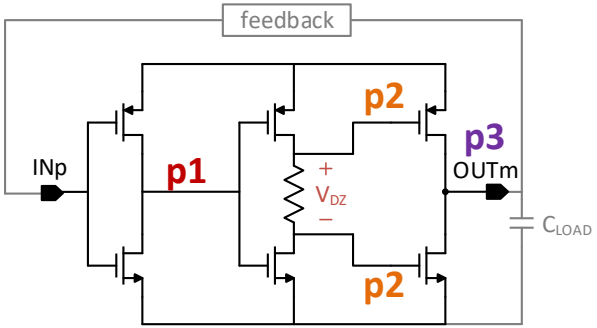


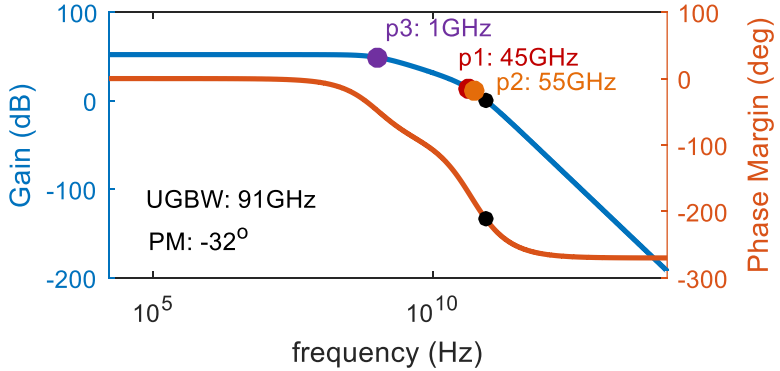
[Lagos, JSSC 2019]

RF-sampling ADC: fast & power efficient channel

Ring amplifier

- Large-signal, transient paradigm
- The simple AC view
  - **Make p1 & p2 as fast as possible**

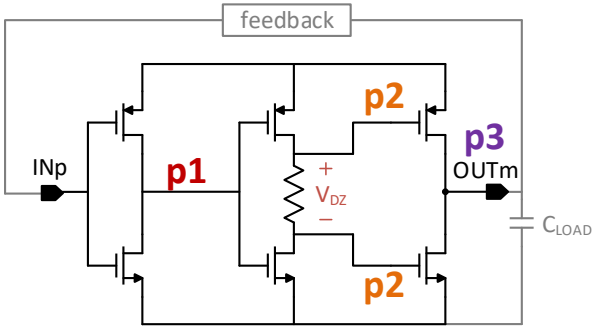


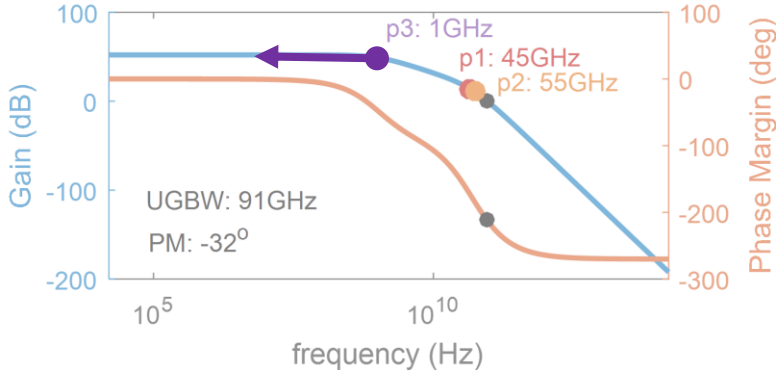


RF-sampling ADC: fast & power efficient channel

Ring amplifier

- Large-signal, transient paradigm
- The simple AC view
  - Make p1 & p2 as fast as possible
  - **Dynamically reduce p3**

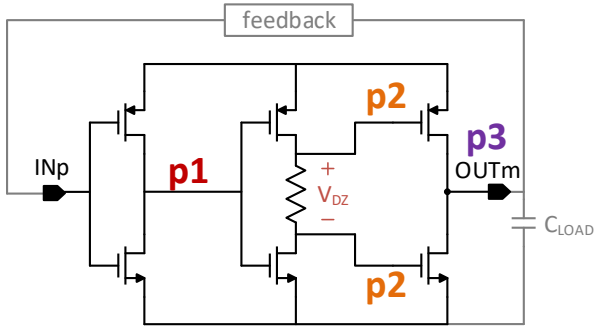


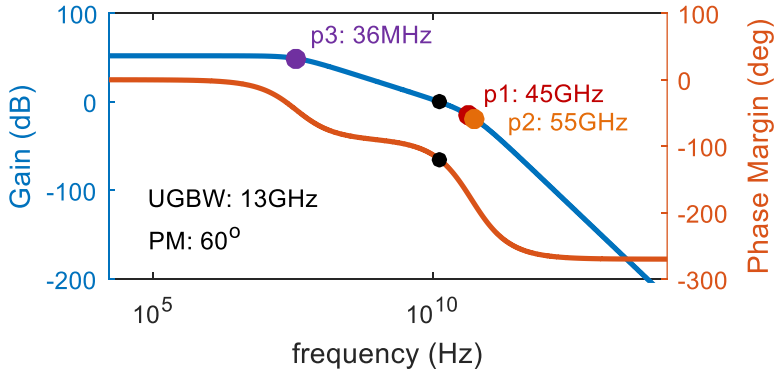


RF-sampling ADC: fast & power efficient channel

Ring amplifier

- Large-signal, transient paradigm
- The simple AC view
  - Make p1 & p2 as fast as possible
  - Dynamically reduce p3
  - **ring oscillator → ring amplifier**

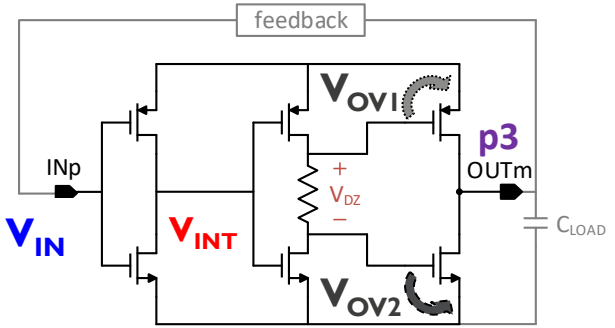




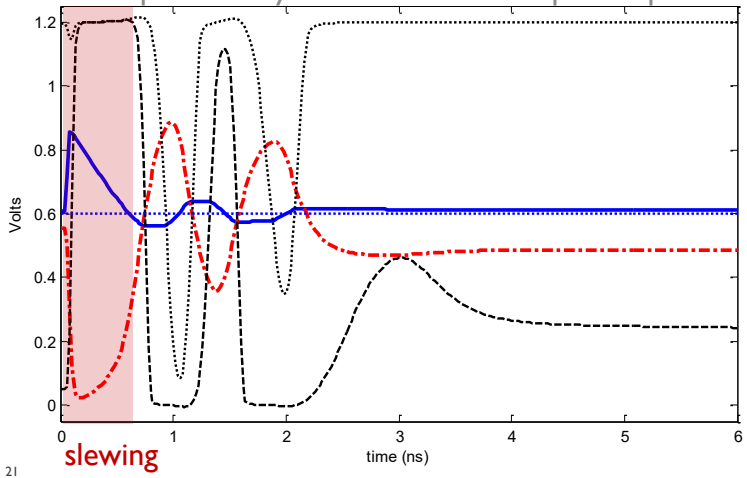
RF-sampling ADC: fast & power efficient channel

Ring amplifier

- Large-signal, transient paradigm
- The simple AC view
  - Make p1 & p2 as fast as possible
  - Dynamically reduce p3
  - ring oscillator → ring amplifier
- The larger DC/transient story
  - **V_{ov} initially huge**
    - Slew-rate at theoretical maximum ☺



Exemplified unity feedback underdamped response

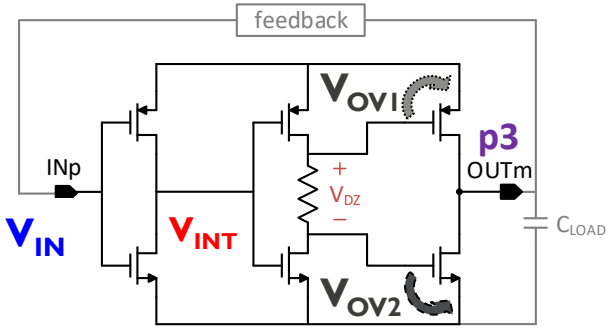


imec

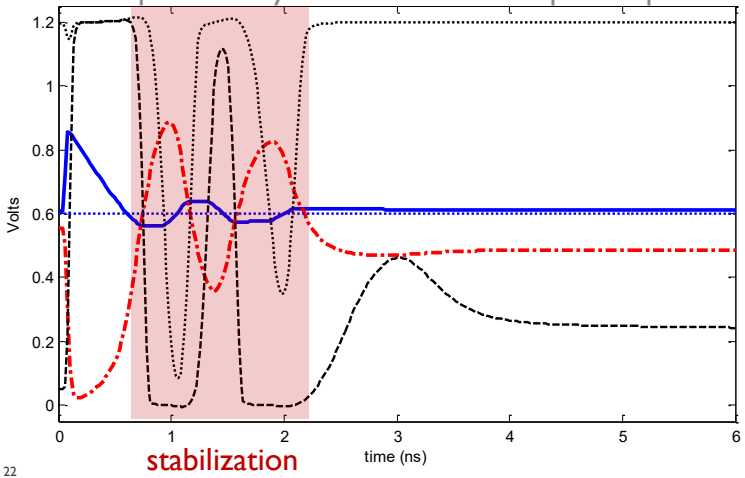
RF-sampling ADC: fast & power efficient channel

Ring amplifier

- Large-signal, transient paradigm
- The simple AC view
  - Make p1 & p2 as fast as possible
  - Dynamically reduce p3
  - ring oscillator → ring amplifier
- The larger DC/transient story
  - V_{OV} initially huge
    - Slew-rate at theoretical maximum ☺
  - **Second stage dead-zone dampens the oscillations → stabilization**
    - **Critically damped response preferred**



Exemplified unity feedback underdamped response



RF-sampling ADC: fast & power efficient channel

Ring amplifier

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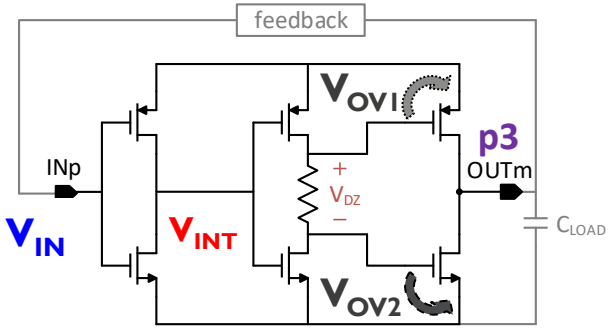
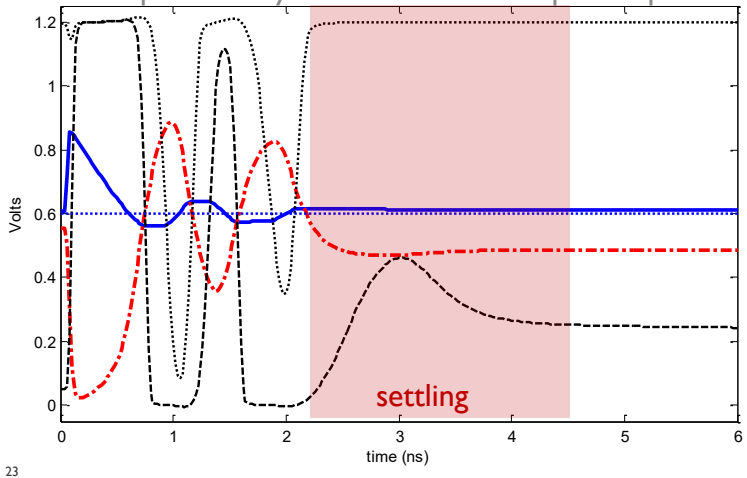
  - ring oscillator → ring amplifier
- The larger DC/transient story
  - V_{OV} initially huge
    - Slew-rate at theoretical maximum ☺
  - **V_{OV} reduced to adjust P3**
    - **Reduces V_{DSAT} → swing/linearity ☺**
    - **Increases r_o → gain/linearity ☺**
    - **Reduces g_m → noise filtering ☺**



Exemplified unity feedback underdamped response

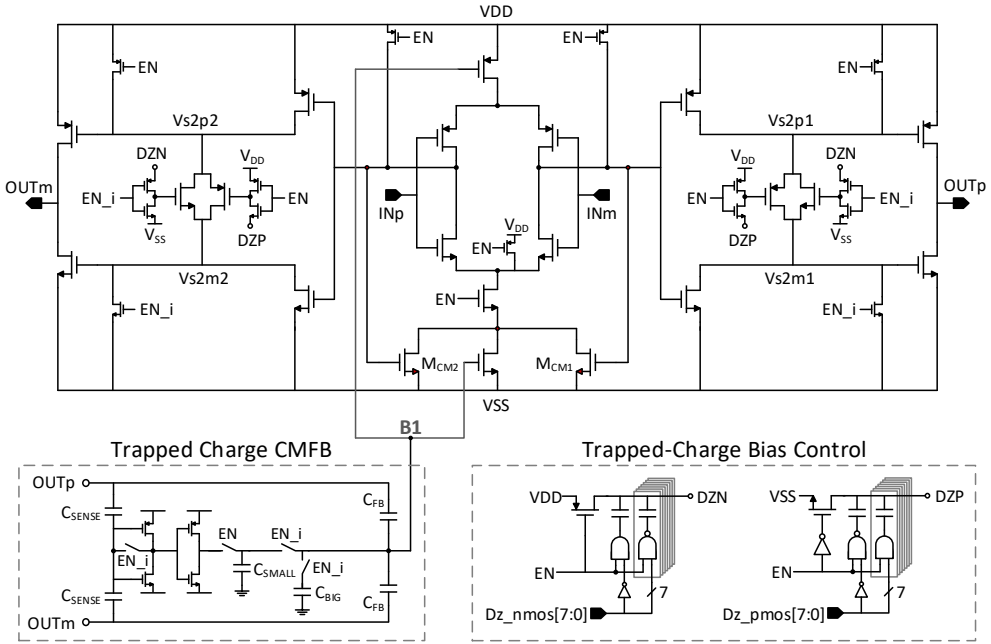


RF-sampling ADC: fast & power efficient channel

Ring amplifier: real implementation

Imec RFs ADC [Hershberg, JSSCC 2021]

System	4 GS/s
Channel	**1 GS/s**
SNDR	62 dB
SFDR	75 dB
Power	75 mW
FoM_W	18 fJ/cs

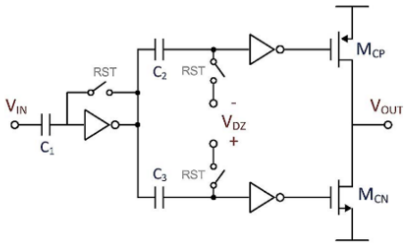


- Order-of-magnitude improvement to SoTA
  - [Hershberg, JSSCC 2021] → 36 amplifiers
  - [Markulic, VLSI 2024] → 144 amplifiers

Bottleneck solved?

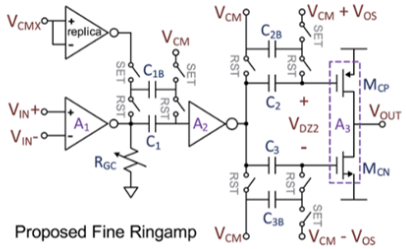
RF-sampling ADC: fast & power efficient channel

Ring amplifier: structural variations



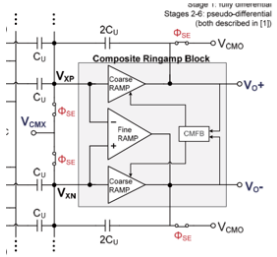
Class-B structure

Hershberg, JSSC Dec. 2012



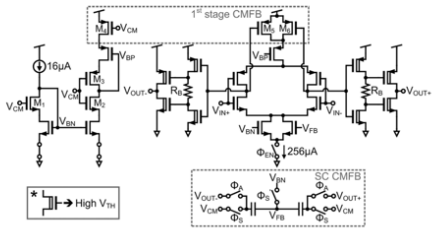
Class-AB structure

Hershberg, VLSI 2013



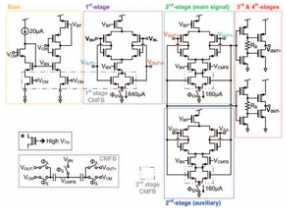
Class-B+AB structure

Hershberg, VLSI 2013



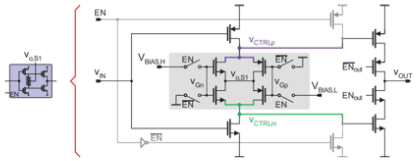
Fully differential structure

Lim, JSSC Dec. 2015



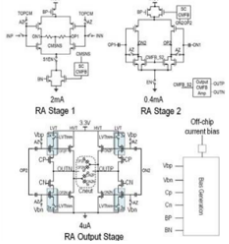
Four-stage structure

Lim, VLSI 2017



Two-stage structure

Lagos, JSSC Feb. 2019

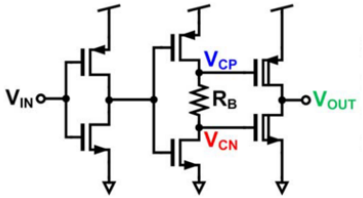


High voltage structure

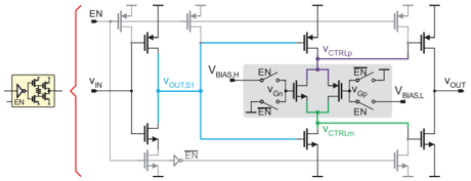
ElShater, ISSCC 2019

RF-sampling ADC: fast & power efficient channel

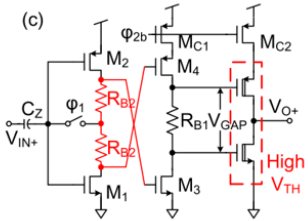
Ring amplifier: enhancements



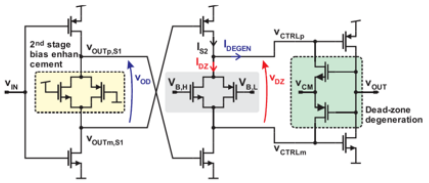
Resistor-based Class-AB
Lim, JSSC Oct. 2015



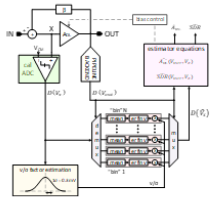
Tunable biasing & power-cycling
Lagos, JSSC Feb. 2019



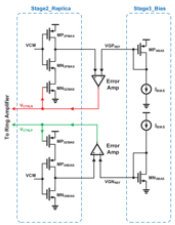
Speed enhancements
Chen, TCASII Nov. 2018
Lagos, JSSC Mar. 2019

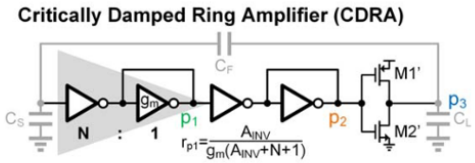


Linearity enhancements
Lagos, JSSC Mar. 2019



Robustness and PVT
Hershberg, ISSCC 2019
Venkatachala, ISCAS 2018
Lim, JSSC Oct. 2015
Lagos, JSSC Feb. 2019





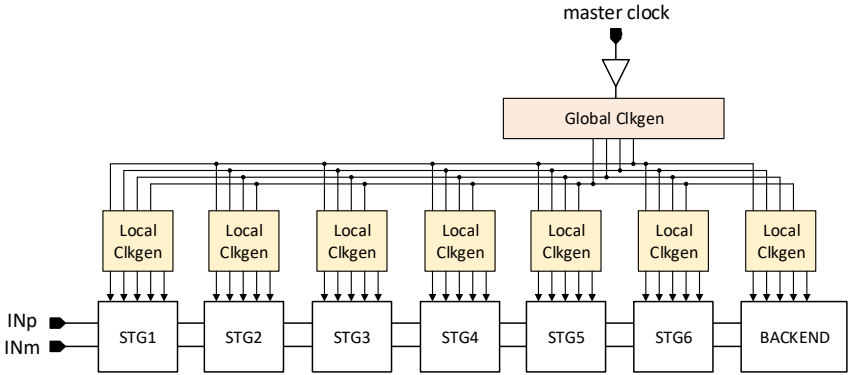
Speed enhancements
Cao ISSCC 2024

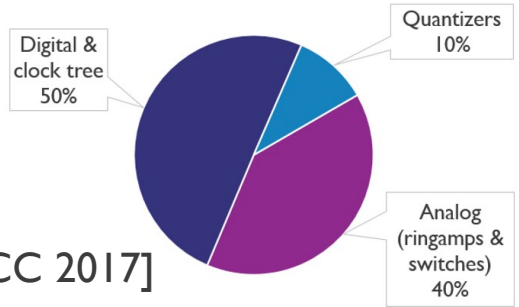
RF-sampling ADC: fast & power efficient channel

Classical clock tree as a power / speed bottleneck

- When ringamps solve amplifier bottleneck, clocking becomes the new bottleneck

- Clock tree in a deep pipeline
  - Many independent branches:
    - Mismatch / Parasitics / Skew
  - Needs timing margin for reliable operation
    - Respect causal timing relationships
    - Guarantee non-overlapping clock phases
  - Exponentially more difficult at high speeds
    - Absolute timing overheads don't scale with relative clock speeds
- Difficult design tradeoffs
  - Power / Speed / Jitter / Reliability





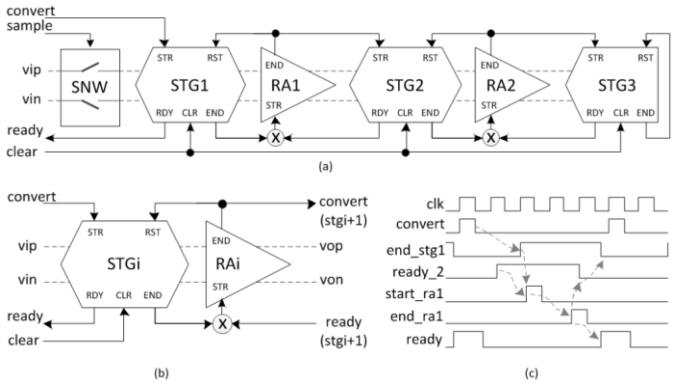
[Lagos, CICC 2017]

RF-sampling ADC: fast & power efficient channel

Classical clock tree as a power / speed bottleneck

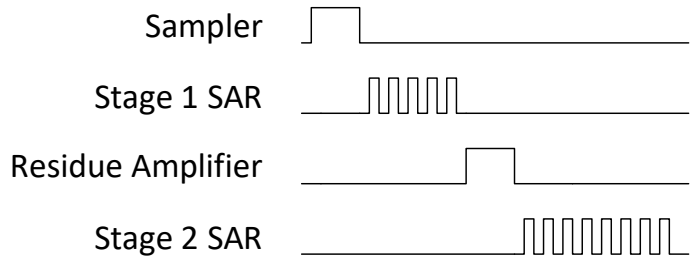
- How to solve it?

- Asynchronous, event-driven timing control …like in SAR ADCs
  - Synchronous SAR requires many *edges* per cycle
    - ☹ Must generate very high-speed clock
  - Asynchronous SAR is a logical/obvious solution
    - ☺ Eliminates high speed clock
    - ☺ More freedom for timing optimization
    - 😐 Must avoid meta-stability



[Vaz, ISSCC 2017]

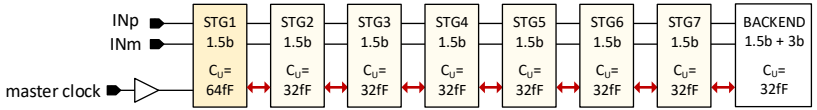
Typical Pipelined-SAR clocking scheme

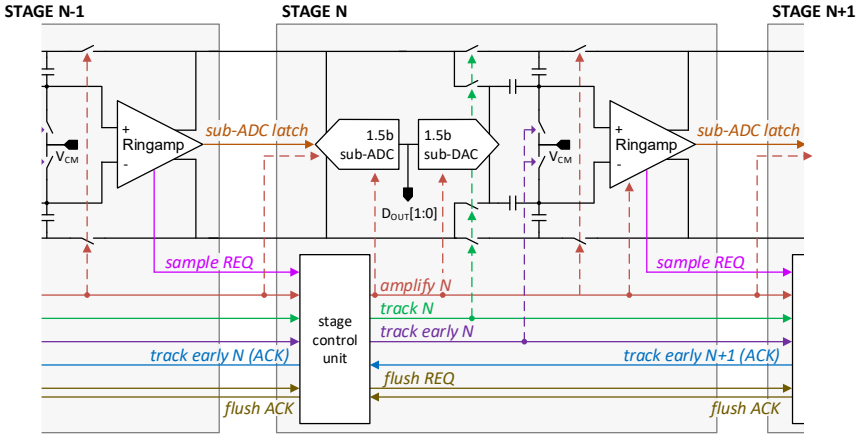


RF-sampling ADC: fast & power efficient channel

Classical clock tree as a power / speed bottleneck

- Asynchronous, event-driven timing control→ applied to *deep* pipelines
- Two parallel paths in a pipeline
  - Analog signal path
  - Digital control clock path
- Digital control path: "Stage Control Units"
  - Finite-state-machine-based
  - Orchestrate stage local-events
  - Communicate to the next/previous stage



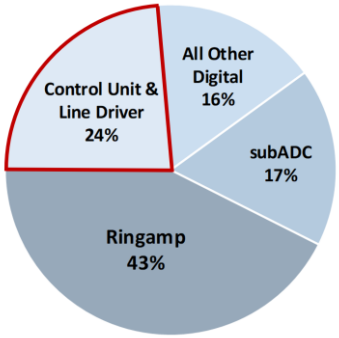


[Hershberg, ISSCC 2019 (2)]

[Hershberg, TICAS1 2021]

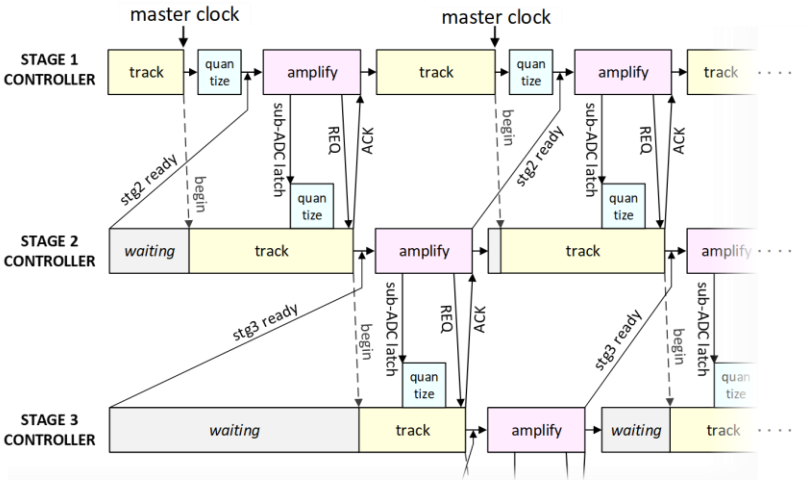
RF-sampling ADC: fast & power efficient channel

Classical clock tree as a power / speed bottleneck



- Key take-away:
  - Synchronous edge-triggered sampling event
  - … then internally asynchronous operation

☺ Minimal global routing
☺ Better for interleaving
☺ Correct-by-construction
☺ Easy reconfigurability (remember Legos?)
☺ Faster (less "wasted" time)
☺ Low power
😐 Verification: handle dead-locks with care



[Hershberg, ISSCC 2019 (2)]

[Hershberg, TICAS1 2021]

2. Signal integrity-preserving hierarchical architecture

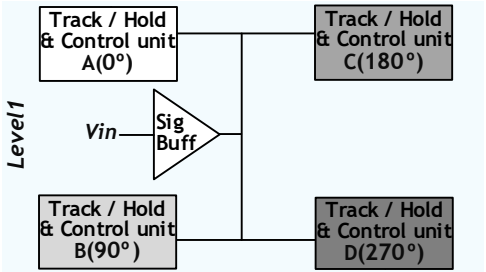
Signal integrity-preserving hierarchical architecture

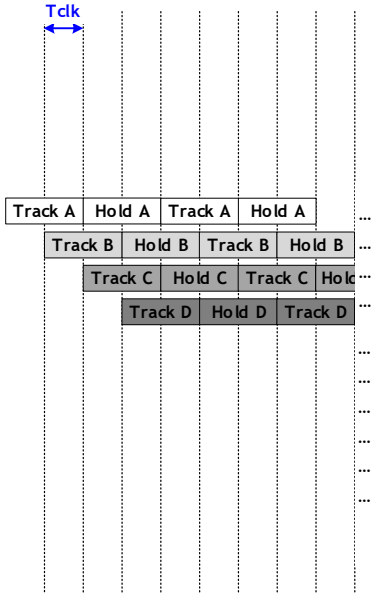
- We explore a >16 GS/s RF-sampling ADC with
  - a **hierarchically interleaved architecture** which efficiently preserves signal integrity and reduces dynamic interleaving calibration effort
  - **Low noise** & **low distortion** at high frequencies

- Higher SNDR & SFDR than any other ADC in SOTA > 12 GSPs
  - Partly reported in [Markulic,VLSI 2024]

Signal integrity-preserving hierarchical architecture

Architecture overview

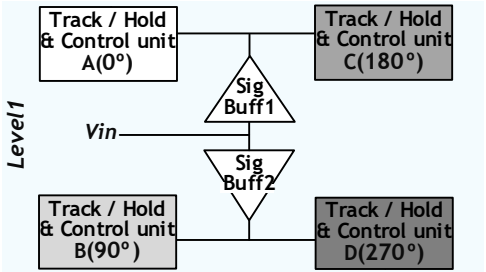


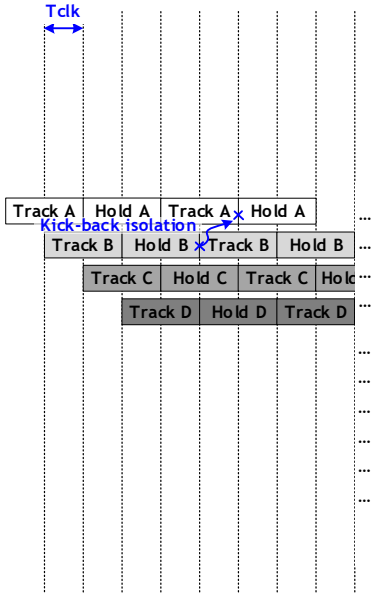


- 4 front-end S&H's.
  - 50 % overlapped track time (2Tclk)

Signal integrity-preserving hierarchical architecture

Architecture overview

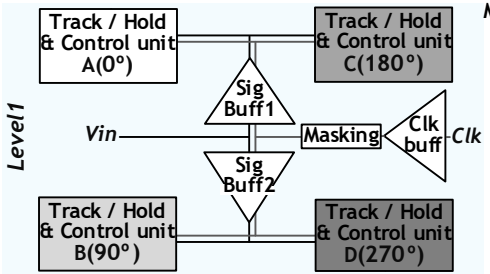


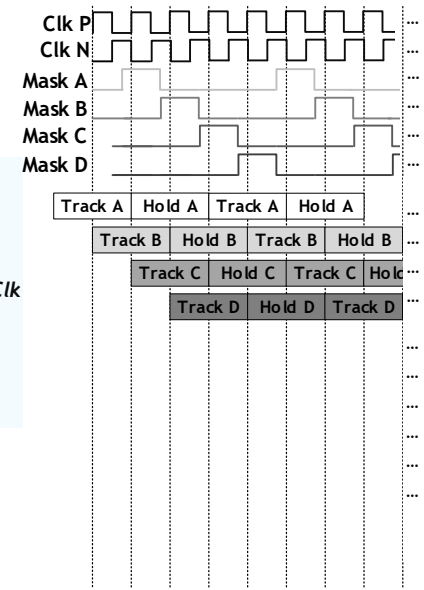


- 4 front-end S&H's.
  - 50 % overlapped track time (2Ts)
- Signal buffer
  - 2 equivalent buffer splits
  - each split always loaded by a *single sampling capacitor* (Cs)
  - kick-back resilience

Signal integrity-preserving hierarchical architecture

Architecture overview

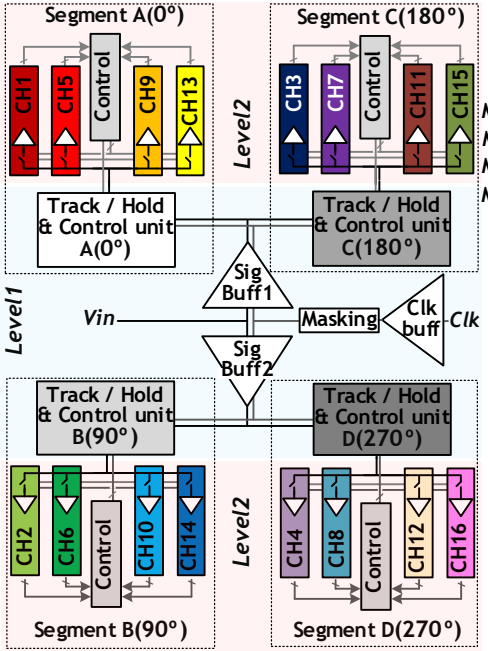


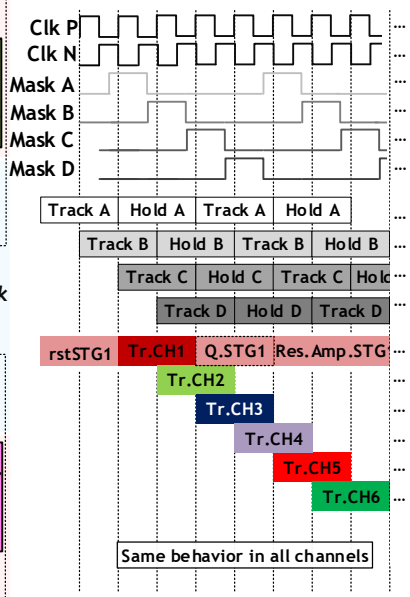


- 4 front-end S&H's.
  - 50 % overlapped track time (2Ts)
- Signal buffer
  - 2 equivalent buffer splits
  - each split always loaded by a *single sampling capacitor* (Cs)
  - kick-back resilience
- 16 GS/s differential clock with *local masking*
  - edge-triggered sampling
  - duty cycle error immunity
- System & layout symmetry
  - Low interleave and even-order distortion

Signal integrity-preserving hierarchical architecture

Architecture overview





- 4 front-end S&H's.
  - 50 % overlapped track time (2Ts)
- Signal buffer
  - 2 equivalent buffer splits
  - each split always loaded by a *single sampling capacitor* (Cs)
  - kick-back resilience
- 16 GS/s differential clock with *local masking*
  - edge-triggered sampling
  - duty cycle error immunity
- System & layout symmetry
  - Low interleave and even-order distortion
- 16 back-end channels (in 4 segments)
  - Asynchronous operation: FSM-based
    - No "deep" clock tree
  - Still a 4-x front-end: limited dynamic interleaving distortion calibration effort

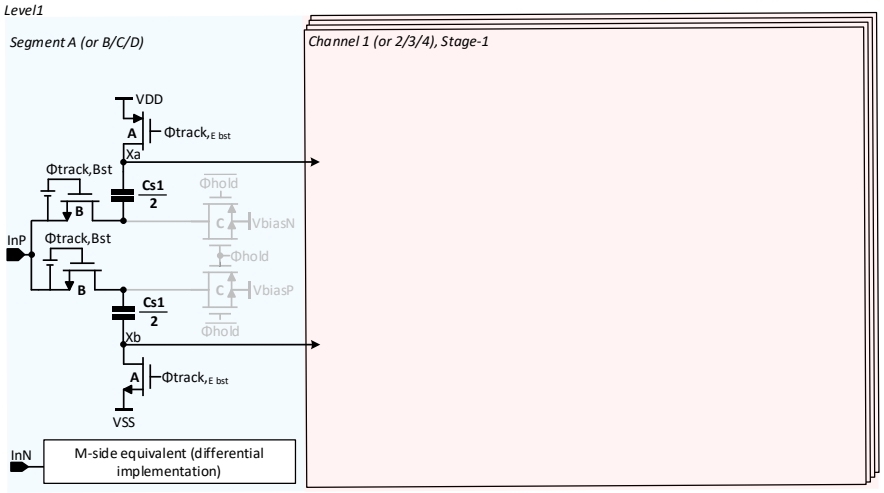
Signal integrity-preserving hierarchical architecture

Hierarchical interface

- How to design the inter-level interface at 4 Gsps at low noise and high linearity?
  - > 70 dB SFDR (without calibration)
  - > 54 ENOB SNR (600 fF sampling capacitor)

Signal integrity-preserving hierarchical architecture

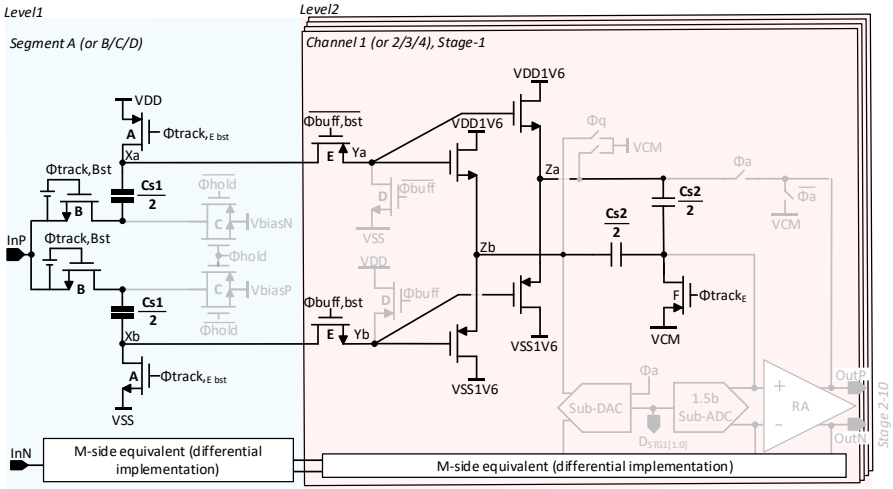
Hierarchical interface **overview**



- ***Level-1*** with 4 front-end samplers
  - 1 shown
- Large linearity:
  - Bottom plate sampling (A)
  - Bootstrapped top plate tracking (B)
- Low noise
  - Large capacitor (600 fF)
  - Differential sampling
- Interface secret: split capacitor

Signal integrity-preserving hierarchical architecture

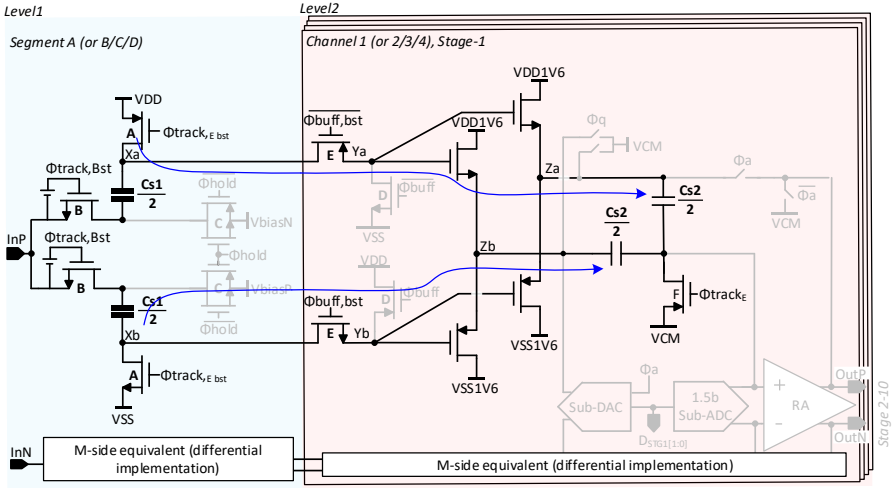
Hierarchical interface **overview**



- ***Level-2*** with 4 back-end samplers
  - 1 shown
- High speed and linearity
  - Dynamic push-pull source follower
  - Bottom plate sampling switch (F)
  - Isolation switch (E)

Signal integrity-preserving hierarchical architecture

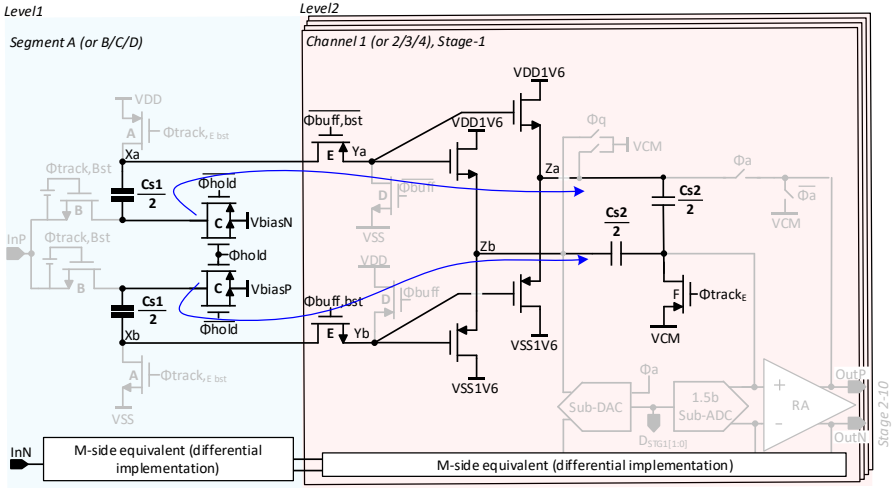
Hierarchical interface **operation (1/5)**



- Operation:
  - Level-1: ***track***
  - Level-2: ***pre-enable***
    - Resets memory effects
    - no "turn-on overhead" in the next phase
    - Other channels isolated by the switch E

Signal integrity-preserving hierarchical architecture

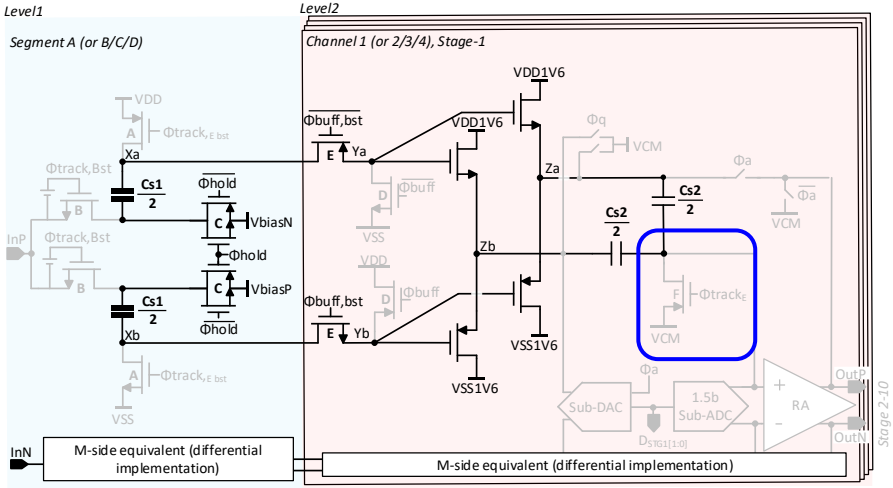
Hierarchical interface **operation (2/5)**



- Operation:
  - Level-1: ***hold***
  - Level-2: ***track***
    - Split Cs1 used for
      - Sampling
      - Buffer biasing
    - Charge transfer commences *momentarily* thanks to buffer pre-activation

Signal integrity-preserving hierarchical architecture

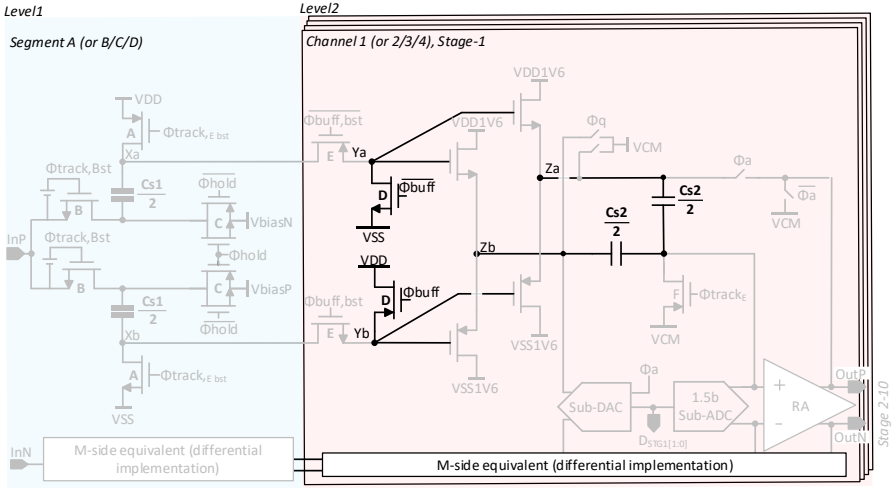
Hierarchical interface **operation (3/5)**



- Operation:
  - Level-1: ***hold***
  - Level-2: ***sample***
    - Bottom switch opens first (F)

Signal integrity-preserving hierarchical architecture

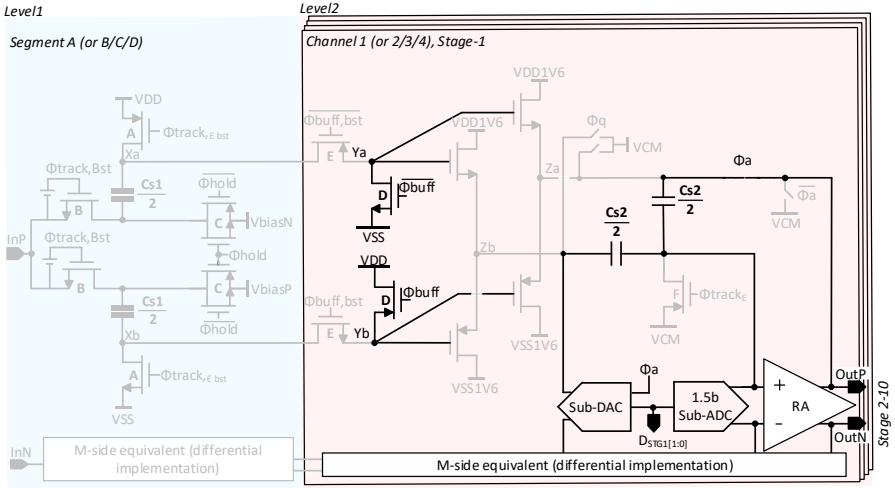
Hierarchical interface **operation (4/5)**



- Operation:
  - Level-1: ***track & hold***
  - Level-2: ***sample***
    - Bottom switch opens first (F)
    - Buffer "opens" to save power
      - Used as top-plate switch
    - E opens to isolate Level-2 from Level-1

Signal integrity-preserving hierarchical architecture

Hierarchical interface **operation (5/5)**



- Operation:
  - Level-1: ***track & hold***
  - Level-2: ***quantization & residue amplification***
  - Rest of the channel is a ringamp-based asynchronous pipeline as described above

3. Wide-band linear front-end buffer

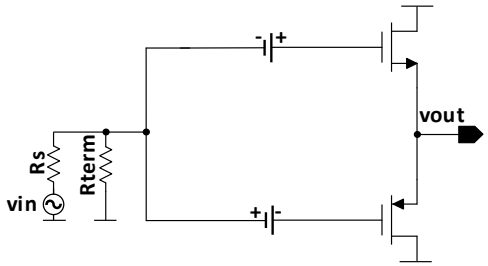
Wide-band linear front-end buffer

Challenge and mission

- > 5GHz bandwidth front-end buffer with
  - > 70 dB SFDR (without calibration)
  - > 54 ENOB SNR (600 fF sampling capacitor)

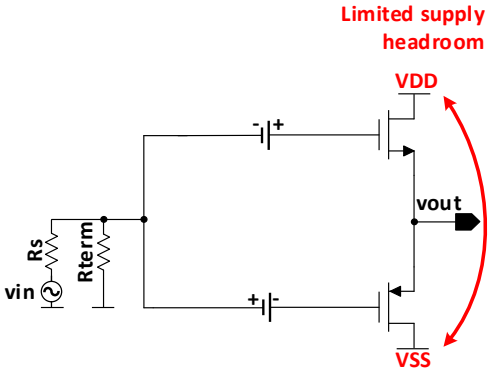
- Without relying on power consuming digital (dynamic) distortion compensation

Wide-band linear front-end buffer



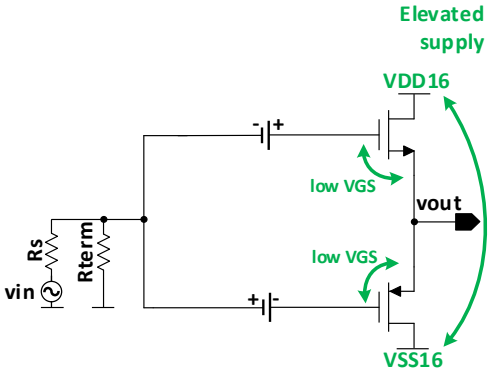
- Push-Pull follower with 2 nonlinearity mechanisms:
  1. Frequency independent
  2. Frequency dependent

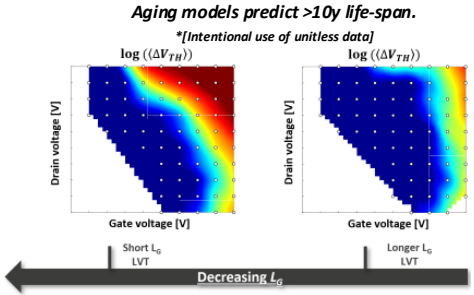
Wide-band linear front-end buffer



- Push-Pull follower with 2 nonlinearity mechanisms:
  1. Frequency independent
     - Limited supply headroom
  2. Frequency dependent

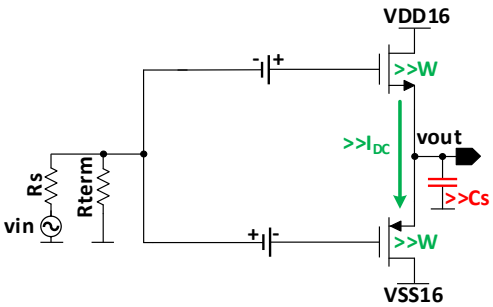
Wide-band linear front-end buffer





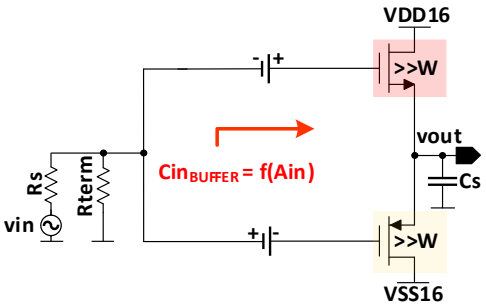
- Push-Pull follower with 2 nonlinearity mechanisms:
  1. Frequency independent
     - Limited supply headroom → solved by supply increase
  2. Frequency dependent

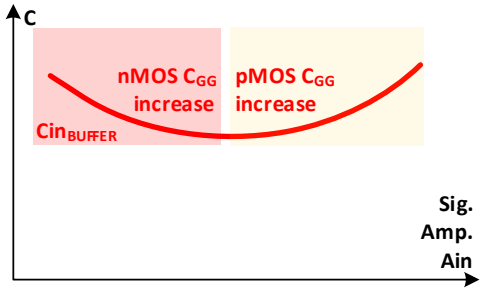
Wide-band linear front-end buffer



- Push-Pull follower with 2 nonlinearity mechanisms:
  1. Frequency independent
     - Limited supply headroom → solved by supply increase
  2. Frequency dependent
     - Slewing at HF with large loads → solved by I_{DC} increase

Wide-band linear front-end buffer

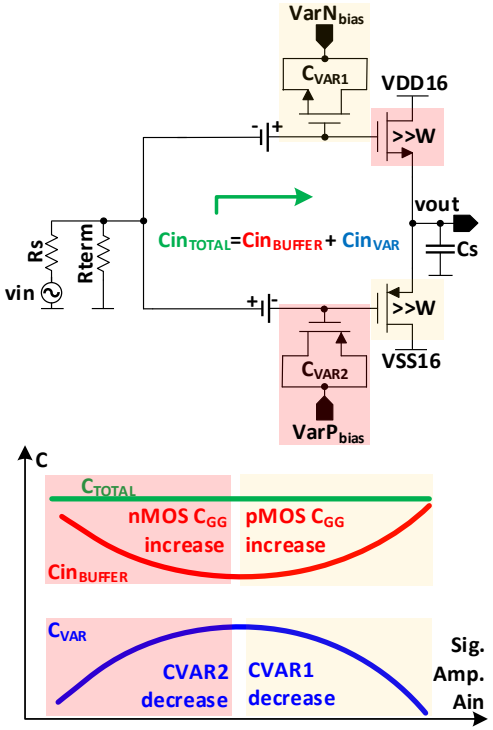




- Push-Pull follower with 2 nonlinearity mechanisms:
  1. Frequency independent
     - Limited supply headroom → solved by supply increase
  2. Frequency dependent
     - Slewing at HF with large loads → solved by I_{DC} increase
     - Signal *amplitude* dependent input loading

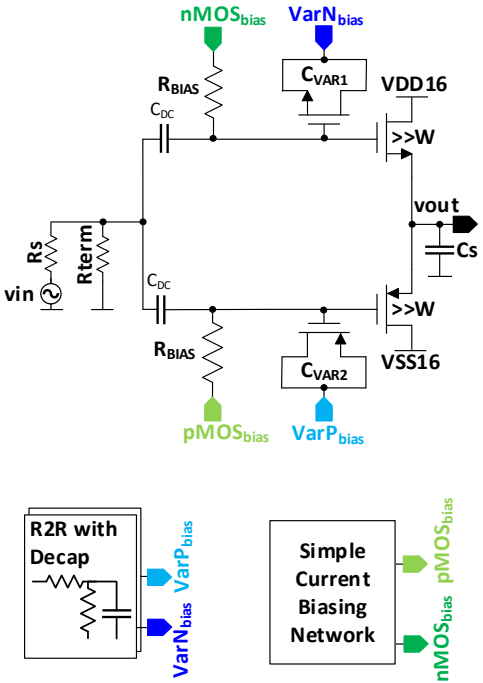
       → *Signal amplitude dependent bandwidth → DISTORTION!*

Wide-band linear front-end buffer



- Push-Pull follower with 2 nonlinearity mechanisms:
  1. Frequency independent
     - Limited supply headroom → solved by supply increase
  2. Frequency dependent
     - Slewing at HF with large loads → solved by I_{DC} increase
     - Signal *amplitude* dependent input loading
- Capacitive neutralization for wide-band linearity
  - Varactor-based
    - nMOS varactor compensates pMOS induced nonlinearity
    - pMOS varactor compensates nMOS induced nonlinearity
  - Simple biasing (high impedance node)

Wide-band linear front-end buffer



- Push-Pull follower with 2 nonlinearity mechanisms:
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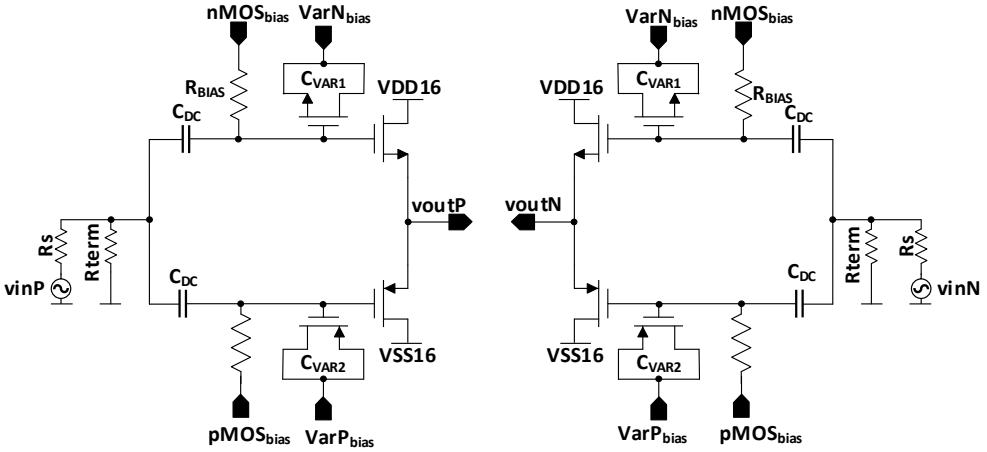
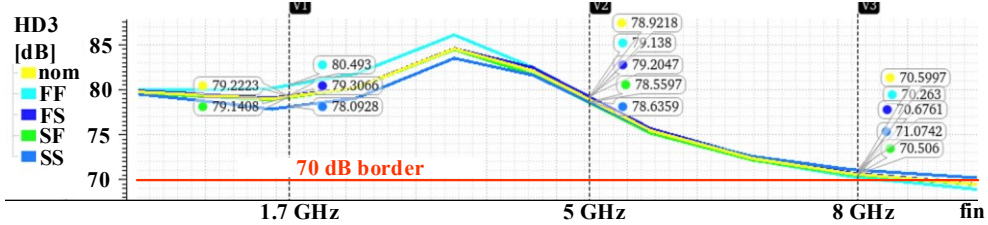
  2. Frequency dependent
     - Slewing at HF with large loads → solved by I_{DC} increase
     - Signal amplitude dependent input loading
- Capacitive neutralization for wide-band linearity
  - Varactor-based
    - nMOS varactor compensates pMOS induced nonlinearity
    - pMOS varactor compensates nMOS induced nonlinearity
  - Simple biasing (high impedance node)
- Current-biased environment for PVT
  - Same flavor transistors share gate terminal connection

Wide-band linear front-end buffer





- Pseudo-differential implementation
- HD3 performance resilient to PVT across a wide-band

Measurements of latest RFs ADC

Measured performance at 16.5 GS/s

Confidential unpublished results

Typical spectrum at low input frequencies

Spectrum at

- Fin = 100 MHz
- Pin = -3dBFs
- Decimated by 4037
- Harmonics labeled by o
- Interleaving spurs x

- 56.6 dB SNDR
- 72 dB SFDR

Measured performance at 16.5 GS/s

Confidential unpublished results

Typical spectrum at high input frequencies

Spectrum at

- Fin = 5000 MHz
- Pin = -3dBFs
- Decimated by 4037
- Harmonics labeled by o
- Interleaving spurs x
  - All interleaving spurs below -75 dBc
- 54 dB SNDR
- 69 dB SFDR – HD3 dominated
  - Negligible even order distortion

Measured performance at 16.5 GS/s

Confidential unpublished results

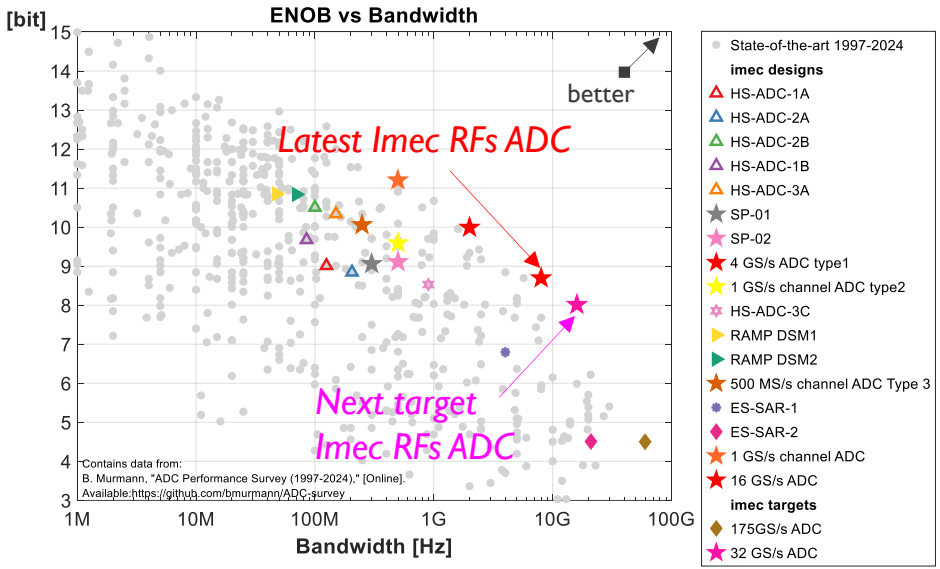
Input/clock frequency sweep at Fclk = 16.5 GS/s & Fin = 250 MHz, respectively

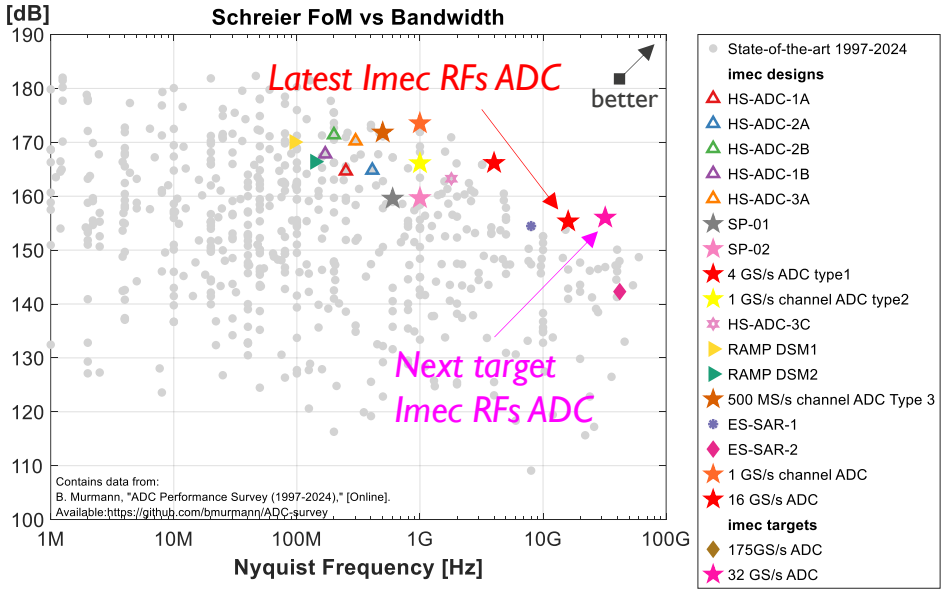
SFDR > 63 dB / SNDR>54 dB / ENOB > 8.7 b across full bandwidth

Measured performance at 16.5 GS/s

Confidential unpublished results

FOMs at the forefront of SOTA





Conclusion

In this talk we discussed the following challenges of RF-sampling ADCs

- Key challenges of RF-sampling ADCs
  1. High speed and efficient channel design
     - Amplification bottleneck
     - Clock distribution bottleneck
  2. Architectural limits
     - Directly interleaving: danger of excessive loading and interleaving distortion
     - Hierarchical interleaving: danger of SNDR degradation at the hierarchy interface
  3. Wide-band linear front-end buffering & sampling

Conclusion

In this talk we discussed the following challenges of RF-sampling ADCs

- Key challenges of RF-sampling ADCs
  1. High speed and efficient channel design
     - Amplification bottleneck → resolved by ringamps
     - Clock distribution bottleneck → resolved by asynchronous operation
  2. Architectural limits
     - ~~Directly interleaving: danger of excessive loading and interleaving distortion~~
     - Hierarchical interleaving: danger of SNDR degradation at the hierarchy interface
       → resolved by split-cap-sampling and push-pull-based active reset / rebuffering
  3. Wide-band linear front-end buffering & sampling → resolved by capacitance neutralization

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Conclusion

Looking to the future …

- Key challenges of next generation RF-sampling ADCs will remain *the same* but…
  - More bandwidth: > 20 GHz BW
  - More linearity: SFDR > 65 dB
  - Higher sampling rates (> 32 Gsps)
  - Less power (Sub 1-mW)

- Will our strategy remain valid?

- Additional opportunities:
  - Availability of nm CMOS with great mixed signal / analog performance
  - Efficient digital linearization of static and dynamic distortion

Thank you.


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